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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Group art unit: 2823
Examiner: Fernando L. Toledo

In Re PATENT APPLICATION of:

Applicant(s): Masaru TAKAISHI

Serial No.: 10/766,212

Filed: January 29, 2004

For: METHOD FOR FILLING A CONTACT HOLE HAVING A SMALL DIAMETER AND A LARGE ASPECT RATIO

Atty. ref.: AI 325

**BRIEF ON APPEAL**

January 22, 2006

**MAIL STOP APPEAL BRIEF - PATENTS**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

## INTRODUCTION

This is an Appeal from a final Office Action mailed on June 30, 2006. This Brief on Appeal is being filed within two months from the date of filing the notice of appeal, and is being filed together with the fee of $500.00 as required by 37 CFR §41.20(b)(2). Should no remittance be attached or if any additional fees are needed, please charge the same to our deposit account number 18-0002 and advise us accordingly.

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The Examiner's final Office Action rejected claims 1-7 and 9, i.e., all of the claims pending in the application. A Request for Reconsideration to the Examiner's final Office Action was filed on October 26, 2006. An Advisory Action was mailed on November 17, 2006, which held that the Request for Reconsideration did not place the application in condition for allowance.

The Notice of Appeal was filed together with the requisite fee on November 28, 2006. A copy of the claims involved in this Appeal is attached as Appendix A.

## REAL PARTY IN INTEREST

The present application has been assigned to Rohm Co., Ltd., of Kyoto, Japan, which is the real party in interest.

## RELATED APPEALS AND INTERFERENCES

To the best of the undersigned attorney's belief and knowledge, no other appeals or interferences are or have been filed which may be related to, directly affect or be directly affected by, or have a bearing on the Board's decision in the pending appeal.

## STATUS OF THE CLAIMS

This application was filed on January 29, 2004, with claims 1-9.

Claim 1 was amended and claim 8 was canceled, with the Amendment filed December 14, 2005.

Claims 1-7 and 9 are pending in the application.

Claims 1-7 and 9 have been finally rejected.

Claims 1-7 and 9 are appealed.

## STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Examiner's final action.

## SUMMARY OF CLAIMED SUBJECT MATTER

Referring generally to Figures 1-3 of the application, and to the specification, Appellant's independent claim 1 is directed to a method for manufacturing a semiconductor device having a semiconductor substrate 1 with a contact hole 4 filled by an aluminum-containing thin film. The method includes forming a silicon-containing thin film 15 in a region having a predetermined area Sp (see Figure 3), including an inner surface of the contact hole 4 on a surface of the semiconductor substrate 1 (see page 15, line 9 through page 16, line 11, as well as Figure 2A and Figure 2B). Appellant's claim 1 further recites forming an aluminum-containing thin film 16 on the surface of the semiconductor substrate 1 on which the silicon-containing thin film 15 is formed (see page 16, line 12 through page 17, line 4, as well as Figure 2C). Additionally, claim 1 recites heating the semiconductor substrate 1 on which the aluminum-containing thin film 16 is formed to such a temperature so as to cause silicon to diffuse with respect to aluminum (see page 16, lines 17-19, and page 17, lines 5-7). This claim also recites that the semiconductor

substrate 1 is provided with a plurality of cells C, each including the contact hole 4 (see Figure 3). Moreover, Appellant's claim 1 recites that the ratio of an amount of silicon contained in the thin film 15 formed in the region having the predetermined area Sp per unit cell C, to the amount of aluminum supplied to a unit cell C in a step of forming the aluminum thin film 16, is not less than 0.1 % and not more than 2 % by atomic ratio (see page 17, line 22 through page 18, line 11). The advantages of this claimed operation are discussed, for example, on page 9, line 25 through page 10, line 5.

## GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-7 and 9 have been anticipated, under 35 U.S.C. §102(b), by *Hsu et al.* (USP 6,143,645).

## ARGUMENTS

1. Rejection under 35 U.S.C. §102(b) over USP 6,143,645, herein after *Hsu et al.*

Claims 1, 2, 3 and 7

Appellant's independent claim 1 recites, *inter alia*, a specific ratio. The ratio is based on an amount of silicon contained in the silicon-containing thin film formed in a region having a predetermined area per unit cell, to an amount of aluminum supplied to a unit cell in the step of forming the aluminum thin film. The ratio is not less than 0.1 percent, and not more than 2 percent by atomic ratio.

*Hsu et al.* is directed to a reduced temperature contact/via filling, which includes, as shown in Figures 2A-2C, an underlying layer 200, having a dielectric layer 210 formed thereon. A via hole 202 is formed in the dielectric layer 210. As shown in Figure 2A, a silicon-rich layer 500 is formed on the dielectric layer 210, and in the via hole 202. The silicon-rich layer 500 is referred to as a wetting layer, and is a silicon-rich titanium silicide layer. This reference also discloses that a diffusion barrier layer 510 can be formed on the surface of the silicon-rich layer 500, and that an aluminum alloy layer 520 is formed on the diffusion barrier layer 510. This reference teaches that the aluminum alloy layer 520 is deposited at a temperature no greater than 400 degrees Celsius, and as shown in Figure 2C1, closes the mouth of the via hole 202. As disclosed in column 3, lines 39-45 of this patent, the aluminum alloy layer 520 is forced into the via hole 202 using high pressure gas. This reference also discloses, in column 4, lines 1-7, that in an experiment, the aluminum alloy layer 520 was deposited using a heater temperature of 450 degrees Celsius, with a wafer temperature of 370 degrees Celsius. Moreover, the Background of the Invention of this patent discloses that it is known to alloy aluminum with a small fraction of silicon, e.g. 1 percent atomic (see column 2, lines 1 and 2). However, the background of this patent further discloses that the use of silicon alloys presents various problems (see column 2, lines 3 and 4). This reference thus discloses utilizing an aluminum alloy, which includes copper (see column 4, lines 2 and 3, as well as column 5, line 49 through column 6, line 59).

The Examiner's Action has contented that the background disclosure of this reference, that is, the disclosure that an aluminum metallization can include a silicon alloy, anticipates Appellant's claimed ratio, and asserts that the metallization 520 would inherently include silicon. However, as noted above, the cited reference specifically discloses that in the various disclosed embodiments that the aluminum alloy is alloyed with copper. There is absolutely no disclosure from this reference that the aluminum alloy 520 includes, either explicitly or inherently, silicon.

It is further respectfully noted that the Examiner is impermissibly modifying the invention disclosed by the cited reference in order to establish his anticipation rejection. That is, even if the cited reference did not disclose that the aluminum alloy includes copper, one would still have to combine the teachings from the Background of the Invention with the disclosed embodiments in order to reach the conclusion presented by the Examiner's Action, that is, that the metallization 520 includes a small fraction of silicon. Thus, the Examiner is impermissibly combining the teachings from the Background of the Invention with the various disclosed embodiments. Moreover, the Background of the Invention does not establish that an aluminum metallization inherently is alloyed with a small fraction of silicon, e.g. 1% atomic, as asserted by the Examiner's Action. In fact, it is noted that the reference teaches away from utilizing silicon alloy, since the reference discloses that silicon alloys present problems, as discussed in columns

2, lines 4 and 5, and further discloses that the aluminum alloy is alloyed with copper, rather than with silicon.

Furthermore, it is additionally noted that Appellant's independent claim 1 is not reciting the amount of silicon contained within the aluminum-containing thin film 16, as the Examiner is apparently interpreting the claim. Instead, this claim is directed to the ratio between the amount of silicon in the silicon-containing thin film 15 to the amount of aluminum supplied during the forming of the aluminum thin film 16. The cited reference does not disclose or suggest any sort of ratio between the silicon rich layer 500 and the aluminum alloy 520, much less the specific ratio recited by Appellant's independent claim 1. It is thus respectfully submitted that the Examiner's Action has failed to establish a *prima facie* case of anticipation against independent claim 1 and dependent claims 2, 3 and 7. It is requested that the Board reverse the Examiner's decision.

Claim 4

Claim 4 further recites the operation of removing the silicon-containing thin film. This particular feature can best be seen in Appellant's Figure 2B. In establishing his anticipation rejection, the Examiner relies on column 7, lines 16 through 19 of the cited reference. These particular passages of the patent disclose that the invention can be adapted to cavity filling utilizing a metal plug. However, there is no disclosure from this reference that any portion of the silicon-rich layer 500, which the Examiner's Action has equated as being a silicon-

containing thin film, is removed in any manner what-so-ever. It is thus submitted that the Examiner's Action has failed to establish a *prima facie* case of anticipation against dependent claim 4. It is requested that the Board reverse the Examiner's decision.

Claim 5

Claim 5 recites that the step of removing the silicon-containing thin film includes using a mask having a predetermined pattern. In rejecting claim 5, the Examiner's Action states that it is conventional in the art to form a plug using a mask to avoid etching the plug. However, it is initially respectfully submitted that it is irrelevant as to what is conventional in establishing a §102 rejection. Instead, the cited reference must disclose, either explicitly or inherently, the claimed invention. Moreover, it is further respectfully submitted that the cited reference does not disclose using a mask having a predetermined pattern. As noted above with respect to the rejection against claim 4, the cited reference does not disclose removing any portion of the silicon-rich layer 500. Moreover, the cited reference does not disclose using a mask having a predetermined pattern, to remove any feature what-so-ever, much less the silicon rich layer 500. It is noted that the reference does disclose etching the dielectric layer 210 to form the via hole 202; however, there is no disclosure that a mask is used. Moreover, even if a mask is used, this still would not anticipate Appellant's claim 5, which recites that a mask is used to remove a silicon-containing thin film. It is submitted that the Examiner's

Action has failed to establish a *prima facie* case of anticipation against claim 5. It is requested that the Board reverse the Examiner's decision.

Claim 6

Claim 6 recites that the step of removing the silicon-containing thin film is done by etching. In rejecting this claim, the Action contends that it is well-known and conventional to remove unwanted portions by etching. However, it is respectfully submitted that it is irrelevant as to what is well-known and conventional in the art in establishing an anticipation rejection. Instead, the cited reference either explicitly or inherently must disclose the claimed invention. However, the cited reference does not disclose that the silicon-rich layer 500 is etched in any manner what-so-ever. As noted above with respect to the rejection against dependent claim 5, the cited reference does disclose that the dielectric layer 210 is etched to form the via hole 202. However, this does not anticipate Appellant's claim 6 which recites that the silicon-containing thin film is etched. It is submitted that the Examiner's Action has failed to establish a *prima facie* case of anticipation against claim 6. It is requested that the Board reverse the Examiner's decision.

Claim 9

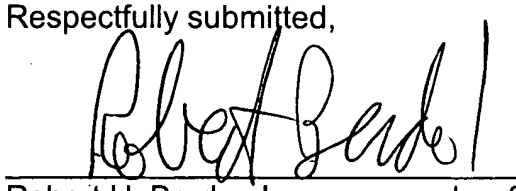
Claim 9 recites that the heating of the semiconductor substrate is at 380 degrees Celsius to 570 degrees Celsius. The Examiner's Action relies on column

4, lines 15-30 of the cited reference in establishing this part of the rejection. However, these passages of this reference only disclose that the sputtering of the aluminum alloy is performed at a temperature that is less than 450 degrees Celsius. There is no disclosure from these passages that the underlying layer 200 (which can be a semiconductor substrate) is heated, much less heated to Appellant's claimed range. Further, it is noted that column 4, lines 5 and 6 of the reference disclose that the wafer temperature can be 370 degrees Celsius during the filling of the vias. However, 370 degrees Celsius is less than Appellant's claimed range of 380 degrees Celsius to 570 degrees Celsius. As such, it is submitted that the Examiner's Action has failed to establish a *prima facie* case of anticipation against dependent claim 9. It is requested that the Board reverse the Examiner's decision.

FINAL CONCLUSION

Appellant has demonstrated that the Examiner's rejections of the claims as being anticipated lack basis in fact and in law. Appellant therefore respectfully requests the Honorable Board of Patent Appeals and Interferences to reverse or withdraw all of the rejections.

Respectfully submitted,



January 22, 2007
Date

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# APPENDIX A

## Pending Claims Appendix

Claim 1 (previously presented): A method for manufacturing a semiconductor device having a semiconductor substrate with a contact hole filled by an aluminum-containing thin film, comprising the steps of:

forming a silicon-containing thin film in a region having a predetermined area including the inner surface of the contact hole on the surface of the semiconductor substrate;

forming an aluminum-containing thin film on the surface of the semiconductor substrate on which the silicon-containing thin film is formed; and

heating the semiconductor substrate on which the aluminum-containing thin film is formed to such a temperature as to cause silicon to diffuse with respect to aluminum;

wherein the semiconductor substrate is provided with a plurality of cells each including the contact hole, and

the ratio of the amount of silicon contained in the silicon-containing thin film formed in the region having the predetermined area per unit cell to the amount of aluminum supplied to a unit cell in the step of forming the aluminum thin film is not less than 0.1% and not more than 2% by atomic ratio.

Claim 2 (original): A method for manufacturing a semiconductor device as claimed in claim 1, wherein the step of forming an aluminum-containing thin film

and the step of heating the semiconductor substrate are carried out simultaneously.

Claim 3 (original): A method for manufacturing a semiconductor device as claimed in claim 1, wherein the step of heating the semiconductor substrate is carried out after completing the step of forming the aluminum thin film.

Claim 4 (original): A method for manufacturing a semiconductor device as claimed in claim 1, wherein the step of forming a silicon-containing thin film in the region having the predetermined area includes the steps of:

forming a silicon-containing thin film in a region larger than the predetermined area; and

removing the silicon-containing thin film so that the area of the silicon-containing thin film can become the abovementioned predetermined area.

Claim 5 (original): A method for manufacturing a semiconductor device as claimed in claim 4, wherein the step of removing the silicon-containing thin film includes a step of removing the silicon-containing thin film using a mask having a predetermined pattern.

Claim 6 (original): A method for manufacturing a semiconductor device as claimed in claim 4, wherein the step of removing the silicon-containing thin film includes a step of removing the silicon-containing thin film by etching.

Claim 7 (original): A method for manufacturing a semiconductor device as claimed in claim 1, wherein the predetermined area is not more than 99% of the area of the aluminum-containing thin film formed in the step of forming the aluminum thin film.

Claim 8 (canceled).

Claim 9 (original): A method for manufacturing a semiconductor device as claimed in claim 1, wherein the step of heating the semiconductor substrate includes a step of heating the semiconductor substrate to 380C° ~ 570 C°.

APPENDIX B

EVIDENCE APPENDIX

None.

# APPENDIX C

## RELATED PROCEEDINGS APPENDIX

None.